REMARKS/ARGUMENTS

Claims 1-14 are pending in the present application. With this amendment, claims 6 and 11 have been canceled; claims 1, 7, 12, and 13 have been amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 6 and 11 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicant regards as the invention. Applicant has canceled claims 6 and 11. Therefore, this rejection has been overcome and should be withdrawn.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 4-6, 12 and 14 under 35 U.S.C. § 102 as being anticipated by *Jaquette* et al., ECC in Memory Arrays Having Subsequent Insertion of Content, U.S. Patent No. 6,009,547, December 28, 1999 (hereinafter "*Jaquette*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claim 6 has been canceled. Therefore, this rejection has been overcome with respect to claim 6.

Applicant's claims 1 and 12 recite similar features. According to Applicant's claims, a plurality of blocks in a first memory is allocated for storing unblocked data. This data is a transfer length of data. As this data is received, it is written into successive blocks until the end of the transfer length is reached. If the end block that includes the end of the transfer length is not full of data, padding is added to the end block until it is complete. Padding is added only to an end block that includes an end of the transfer length.

As data is being written into a block, a running cyclical redundancy code is calculated for the block. When writing to the block is completed, a final value of the running cyclical redundancy code that was calculated for the block is stored as a first cyclical redundancy code in a second memory on the buffering device.

Jaquette teaches a memory system that receives data and formats the data into blocks of data. After the data has been formatted into blocks of data, an ECC check symbol is calculated for each block. The data and ECC check symbols for each block are then stored in a memory array in separate locations.

Applicant claims allocating blocks of storage for storing a transfer length of data. In contradistinction, *Jaquette* teaches formatting the data into blocks. *Jaquette* does not teach allocating blocks of storage. While *Jaquette* uses the term "blocks", the term is not used in the same way as it is

used by Applicant. Because *Jaquette* does not teach allocating blocks of storage for storing a transfer length of data, *Jaquette* does not anticipate Applicant's claims.

Applicant claims writing the data to these blocks of storage as the data is received. The data is written until the end of the data is reached. If the end block is not full of data, padding is added to the end block until the end block is complete. In *Jaquette*, the data is stored in the memory array after it is formatted into blocks. *Jaquette* does not teach writing data as the data is received. In *Jaquette*, the data is received, formatted, and then written to the memory array. Because *Jaquette* does not teach writing data as data is received, *Jaquette* does not anticipate Applicant's claims.

Applicant also claims calculating a running cyclical redundancy code for each block as data is being written to each block. In contradistinction, *Jaquette* waits until the data is formatted into blocks and then calculates a final ECC check symbol for the entire block of data. This ECC check symbol is not a running ECC check symbol. This ECC check symbol is not calculated as data is being stored.

> The blocks of the data file are supplied to memory manager 18 and byte level ECC check symbols are calculated by CRC generator 20 for a plurality of the blocks, specifically a multiple number (m) of the blocks. The sequence of blocks may be termed a partition, so that the length of the partition (k) equals the multiple times the block length (m)*(l). For example, the partition may comprise 4 blocks (m) and have a total length (k) of 4*32 bytes=128 bytes.

Jaquette et al., column 4, lines 53-61.

Jaquette does not calculate a running ECC check symbol. *Jaquette* does not calculate the ECC check symbol as the data is being written to the memory array. Therefore, *Jaquette* does not anticipate Applicant's claims.

According to Applicant's claims, when writing to each one of the blocks is complete, a final value of the running cyclical redundancy code that was calculated for each block is stored as a first cyclical redundancy code. In *Jaquette*, an ECC check symbol is calculated after the data is formatted. *Jaquette* does not teach calculating a running cyclical redundancy code. *Jaquette* does not teach calculating a running cyclical redundancy code as data is being written. *Jaquette* does not teach storing the final value of the running cyclical redundancy code as a first cyclical redundancy code when writing the data is complete. Therefore, *Jaquette* does not anticipate Applicant's claims.

Jaquette does not anticipate Applicant's claims because *Jaquette* does not teach allocating a plurality of blocks of storage for storing a transfer length of data, writing data to successive blocks as the data is received, calculating a running cyclical redundancy code for each block as data is written to each block, or for each block of storage, storing a final value of the running cyclical redundancy code that was calculated for each block as a first cyclical redundancy code. The remaining claims depend from the independent claims discussed above and are patentable for the reasons given above.

III. **35 U.S.C. § 103, Obviousness**

The Examiner has rejected claims 2 and 13 under 35 U.S.C. § 103(a) as being unpatentable over *Jaquette* in view of *Hogan* et al., Method and Apparatus for Discouraging Duplication of Digital Data, U.S. Patent No. 6,765,739, July 20, 2004 (hereinafter "*Hogan*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicant's claims 2 and 13 recite similar features. Claim 2 recites "wherein the data is received with a protection code that is checked and discarded". The examiner relies on *Hogan* to teach this feature.

The combination of *Jaquette* and *Hogan* does not render claims 2 and 13 obvious because the combination does not teach allocating a plurality of blocks of storage for storing a transfer length of data, writing data to successive blocks as the data is received, calculating a running cyclical redundancy code for each block as data is written to each block, or for each block of storage, storing a final value of the running cyclical redundancy code that was calculated for each block as a first cyclical redundancy code in combination with wherein the data is received with a protection code that is checked and discarded.

The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over *Jaquette* in view of *PCTechGuide* (hereinafter "*PCTechGuide*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claim 3 recites wherein said buffering device is a DDR device connected between a bus and a tape drive. The combination of *Jaquette* and *PCTechGuide* does not render Applicant's claim 3 obvious because the combination does not teach allocating a plurality of blocks of storage for storing a transfer length of data, writing data to successive blocks as the data is received, calculating a running cyclical redundancy code for each block as data is written to each block, or for each block of storage, storing a final value of the running cyclical redundancy code that was calculated for each block as a first cyclical redundancy code in combination with wherein said buffering device is a DDR device connected between a bus and a tape drive.

The Examiner has rejected claims 7-8 and 10-11 under 35 U.S.C. § 103(a) as being unpatentable over *Jaquette* in view of *Malakapalli* et al., Mass Storage Error Correction and Detection System, Method and Article of Manufacture, U.S. Patent No. 6,467,060, October 15, 2002 (hereinafter "*Malakapalli*"). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claim 11 has been canceled. Therefore, this rejection has been overcome with respect to claim 11.

The examiner states that *Jaquette* teaches the features of claim 7 but does not teach the device comprising a comparator connected to compare the second cyclical redundancy code with the first cyclical redundancy code when the fixed size blocks were written. The examiner relies on *Malakapalli* to teach this feature.

Applicant's independent claim 7 recites a plurality of blocks that have been allocated for storing a transfer length of unblocked data; the data being written to successive ones of the plurality of blocks as the data is received until an end one of the transfer length is reached; the cyclical redundancy code engine calculating a running cyclical redundancy code for each of the plurality of blocks as data is written to each one of the plurality of blocks; and a second random access memory for storing a final value of the running cyclical redundancy code that was calculated for each one of the plurality of blocks as a first cyclical redundancy code when writing to each one of the plurality of blocks is completed.

As discussed above, *Jaquette* does not teach a plurality of blocks that have been allocated for storing a transfer length of data, writing data to successive blocks as the data is received, calculating a running cyclical redundancy code for each block as data is written to each block, or for each block of storage, storing a final value of the running cyclical redundancy code that was calculated for each block as a first cyclical redundancy code. Because *Malakapalli* does not teach these features, *Malakapalli* does not cure the deficiencies of *Jaquette*. Therefore, the combination of *Jaquette* and *Malakapalli* does render Applicant's claims obvious.

The remaining claims depend from claim 7 and are patentable for the reasons given above.

The Examiner has rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over *Jaquette* and *Malakapalli* and further in view of *Hogan*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Claim 9 recites "a protection module connected to said first port for checking a protection code that is received and discarding said protection code". The examiner relies on the combination of *Malakapalli* and *Hogan* to teach this feature.

The combination of *Jaquette*, *Malakapalli*, and *Hogan* does not render Applicant's claims obvious because the combination does not teach a plurality of blocks that have been allocated for storing a transfer length of data, writing data to successive blocks as the data is received, calculating a running cyclical redundancy code for each block as data is written to each block, or for each block of storage, storing a final value of the running cyclical redundancy code that was calculated for each block as a first cyclical redundancy code in combination with a protection module connected to said first port for checking a protection code that is received and discarding said protection code.

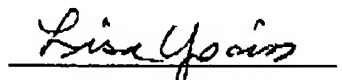
IV. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: November 17, 2006

Respectfully submitted,



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